control semiconductor chip each mounted directly on an electrically conductive heat sink, wherein said power semiconductor chip comprises a Silicon-On-Insulator (SOI) device and said control semiconductor chip comprises a bulk technology semiconductor device having no insulating layer between a device layer and a substrate thereof, and having said substrate connected to ground potential, and said power semiconductor chip and said control semiconductor chip are directly mounted on said electrically conductive heat sink without the use of a separate electrical insulation layer.

REMARKS

In the outstanding Final Official Action, claims 1-7 were rejected under 35 U.S.C. §103(a) as being unpatentable over Takagi et al in view of Lauffer et al and the admitted Japanese prior art, for the reasons of record. In response to Applicants' prior arguments, it was suggested that claim 1 does not expressly recite the argued limitation. In response, claim 1 is herewith amended in order to more clearly and precisely define the instant invention, and it is respectfully submitted that claim 1, as herein amended, and the remaining claims depending therefrom, are clearly patentably distinguishable over the cited and applied art, for the reasons detailed below.

With regard to the suggestion that claim 1 does not expressly recite the argued limitation, it is Applicants' understanding that the recitation of a bulk technology semiconductor would imply this limitation. However, in the interest of advancing prosecution, claim 1 has been amended in order to more positively and expressly recite that the bulk technology semiconductor device has no insulating layer between a device layer and a substrate thereof. Accordingly, it is respectfully requested that this limitation be afforded patentable weight in examining claim 1.

Additionally, claim 1 has been amended in order to positively and precisely recite that both the power semiconductor chip and the control semiconductor chip are each mounted directly on an electrically conductive heat sink. It is respectfully submitted that claim 1, as here in amended as discussed above, is now clearly patentably distinguishable over the cited and applied art.

More particularly, in the cited figure of Takagi, all of the semiconductor devices mounted to the conductor 81 have an intervening insulating layer (10, 80) between the device layer and the substrate, a teaching which is directly contrary to the structure recited in claim 1 as herein amended. The cited Japanese reference shows a different prior-art technique in which a bulk semiconductor type device is mounted on an electrode, which is in turn mounted on an insulating ceramic plate, which is in turn

mounted on the heat sink. Yet another approach is employed in Lauffer, wherein one chip is fastened directly to a conductive plate, and a second chip using conventional technology is indirectly fastened to the conductive plate through a complex plurality of conductive and insulating layers (121, 125, 17, 144 and 14 in Fig. 4), thus resulting in a substantially more complex and expensive device configuration. Furthermore, as noted above, claim 1 has been amended in order to more positively and clearly recite that in the instant invention both semiconductor chips are mounted directed on the electrically conductive heat sink, a clear improvement over Lauffer, which employs several different layers between one of the chips and the substrate.

It is thus clear that the three cited and applied references each show a different prior-art solution, none of which is as simple, compact and elegant as that of the instant invention. It is therefore respectfully submitted that claim 1, as herein amended in order to more clearly and positively recite the foregoing distinctions, and the remaining claims depending therefrom, are clearly patentably distinguishable over the cited and applied art.

Accordingly, entry of this amendment, reconsideration of the rejection of the claims over the references cited, and allowance of this application are earnestly solicited.

Respectfully submitted,

By_____
Steven R. Biren, Reg. No. 26,531
Attorney
(914) 333-9630

CERTIFICATE OF MAILING

It is hereby certified that this correspondence is being deposited with the United States Postal Service as first-class mail in an envelope addressed to:

COMMISSIONER OF PATENTS AND TRADEMARKS
Washington, D.C. 20231

On 10/23/01
(Date of Mailing)

By_____
Steven R. Biren, Reg. No. 26,531

APPENDIX

Amended Claim 1

1. (twice amended) A multiple semiconductor chip (multi-chip) module, comprising at least a power semiconductor chip and a control semiconductor chip each mounted directly on an electrically conductive heat sink, wherein said power semiconductor chip comprises a Silicon-On-Insulator (SOI) device and said control semiconductor chip comprises a bulk technology semiconductor device having no insulating layer between a device layer and a substrate thereof, and having ~~a~~ said substrate connected to ground potential, and said power semiconductor chip and said control semiconductor chip are directly mounted on said electrically conductive heat sink without the use of a separate electrical insulation layer.